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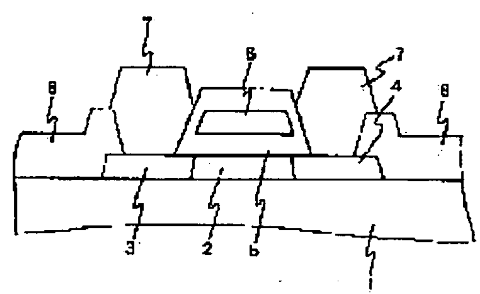
(54) LASER ANNEALING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a large carrier mobility, by orienting specific surface of a poly-Si layer constituting a TFT which is a semiconductor device formed on an insulating substrate, such as a glass substrate, etc.
SOLUTION: After a surface protective film is deposited on a glass substrate 1 by on atmospheric pressure CVD method while the substrate 1 is maintained at 480° C, poly-Si films 2, 3, and 4 are obtained by receystallizing an LPCVD film by projecting ultraviolet pulse laser light using XeC as a gas source upon the LPCVD film from the upper surface of the protective film. When the intensity of the laser light is adjusted to ≥400 mJ/cm2, the principal preferred orientation of the poly-Si film becomes (111). Then, after an SiO2 film formed as the surface protective film is removed a photoetching process is performed for forming the poly-Si films 2, 3, and 4 recrystallized by the laser light in island- like shapes, an SiO2 film 5 for gate insulating film is deposited by the atmospheric pressure CVD method. Consequently, a thin film semiconductor device having large carrier



mobility can be obtained.

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CLAIMS

[Claim(s)]
[Claim 1] The laser annealing approach characterized by considering as the polycrystalline silicon film which has the orientation which made {111} sides the subject for this semi-conductor layer by laser radiation in the thin film semiconductor device which has the semi-conductor film formed on the insulating substrate and this substrate.
[Claim 2] The laser annealing approach characterized by considering as the polycrystalline silicon film with the orientation which made {111} sides the subject by forming the polycrystalline silicon film with a reduced pressure CVD method at the substrate temperature of 550 degrees C or less on an insulating substrate in the laser annealing approach according to claim 1, and carrying out laser radiation of this polycrystalline silicon film.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the laser annealing approach in thin film semiconductor device manufacture, especially relates to the suitable laser annealing approach for the display of an active matrix.
[0002]
[Description of the Prior Art] In recent years, the polycrystalline silicon (Polycrystalline Silicon, omitting poly-Si) which is the point of high-definition-izing as a thin film transistor (Thin Film Transistor, omitting TFT) ingredient which is a thin film semiconductor device for active matrices, and is excellent is used. This Poly-Si film is created by the reduced pressure CVD method (LPCVD law) and the ordinary pressure CVD method (APCVD law). As an insulating substrate, quartz glass or the usual glass plate is used. Since there is big constraint of about 640 degrees C in a maximum temperature in case the usual glass plate is used, the method of recrystallizing by not having thermal effect on a glass plate, but carrying out laser radiation only of the surface layer of the Poly-Si film is tried. According to this approach, crystallinity is improving compared with low warm temperature annealing which does not affect a glass plate.
[0003] The method of irradiating an ultraviolet radiation pulse laser with a big absorption coefficient by Si film like a publication as this laser radiation approach conventionally at JP,60-245124,A, and manufacturing a semiconductor device was examined.
[0004]
[Problem(s) to be Solved by the Invention] With the above-mentioned conventional technique, the carrier mobility when the stacking tendency of the crystal of the Poly-Si film which recrystallized although the TFT property was raised by raising crystallinity by laser radiation not being examined, but creating TFT may have been raised further.
[0005] The object of this invention is to obtain still bigger carrier mobility by taking into consideration the structure of the thin film semiconductor device for raising the property of a thin film semiconductor device, and the stacking tendency of the Poly-Si film especially used for the active layer of TFT.
[0006]
[Means for Solving the Problem] It is attained by giving the orientation which made {111} sides the subject for the Poly-Si layer which constitutes TFT which is the semiconductor device formed on insulating substrates, such as a glass substrate, in the above-mentioned object.
[0007] This Poly-Si layer is 200 mJ/cm2 with Si film which deposited in thickness 1500A or less in temperature with a substrate temperature of 550 degrees C or less with the reduced pressure CVD method, and was deposited below 500 degrees C. With Si film deposited at 520-550 degrees C, they are 400 mJ/cm2 above. It is obtained by irradiating a laser beam from a Poly-Si layer side by the above optical reinforcement. Moreover, when Si film deposited at 550 degrees C is thin-film-ized, at

800-1500A thickness, they are 400 mJ/cm2. At 600-800A thickness, they are 300 mJ/cm2 above. At thickness 600A or less, they are 200 mJ/cm2 above. It is obtained by irradiating a laser beam from a Poly-Si layer side by the above optical reinforcement.

[0008] During Si crystal of each [film / which recrystallized by laser radiation / Poly-Si], it is few, an electronic trap is large to a grain boundary, and a defect is influenced. The phase-boundary-charge consistency of the grain boundary of Poly-Si is each crystal face of Si single crystal, and SiO2. The same relation is materialized and the trap consistency of the film and a perpendicular direction (the <111> directions) serves as size compared with the Poly-Si film with which a stacking tendency is not seen by the Poly-Si film of {111} dominance orientation as a phase-boundary-charge consistency increases in order of <100>, <110>, and <111>. If as parallel as the film, the Poly-Si film of {111} dominance orientation will show a low trap consistency reversely relatively compared with the Poly-Si film with which a stacking tendency is not seen. The depletion-layer width of face produced on the grain community where a trap consistency is low becomes narrow, and a potential barrier here becomes low. The carrier mobility of Poly-Si is decided mainly by the height of the potential failure in a grain boundary. The carrier of TFT flows to the Poly-Si film and a parallel direction. By the Poly-Si film of these conditions to {111} dominance orientation, the mobility of a carrier becomes large relatively compared with Poly-Si without a stacking tendency.

[0009]

[Embodiment of the Invention] The example of this invention is explained below.

[0010] Drawing 1 shows the cross-section structure of the whole TFT which used this invention. A substrate 1 is a glass substrate with a distorted temperature of about 640 degrees C. A substrate 1 is kept at 550 degrees C, and the LPCVD film is made to deposit on condition that pressure 1Torr by using as a raw material the mono-silane gas diluted with helium to 20%. Assembly time makes the 1500A film deposit in 85 minutes. Next, a substrate 1 is kept at 480 degrees C, and 1000A of surface protective coats is made to deposit in about 8 minutes by ordinary pressure CVD by using as a raw material the mono-silane gas and oxygen which were diluted with helium to 4%. The LPCVD film is recrystallized by irradiating the ultraviolet radiation pulse laser (wavelength of 308nm, 25ns of pulse width) which made XeCl the source of gas from the top face of this film, and the Poly-Si film 2, 3, and 4 is obtained. At this time, it is laser beam reinforcement 400 mJ/cm2 The main orientation of the Poly-Si film turns into {111} dominance orientation by considering as the above, and the diameter of average crystal grain is about 1000A. Next, SiO2 used as a surface protective coat The water solution of fluoric acid removes the film. It is SiO2 for gate dielectric film by the ordinary pressure CVD method after letting the process of photoetching which forms the Poly-Si film which recrystallized by laser radiation in the shape of an island pass. The film 5 is made to deposit. Next, 3500A of Poly-Si film 6 for gate electrodes is made to deposit on condition that 550 degrees C and 1Torr. A phot and after sleeping together, IMPURA of the source and the drain fields 3 and 4 is performed for the gate film 5. Conditions are the dose of 5x1015cm-2, and the electrical potential difference of 30KeV using Lynn (P). 5000A of passivation film 8 which consists of phosphorus glass is made to deposit at 480 degrees C, and it is N2 further. They are heat treatment of 20 hours or more, or 200 mJ/cm2 at 600-degree C conditions inside. An in plastic field is activated by irradiating an ultraviolet radiation pulse laser by the above optical reinforcement. TFT is formed by carrying out 6000A spatter of the aluminum electrode 7 the phot for contact, and after a dirty stroke.

[0011] With a reduced pressure CVD method, drawing 2 makes substrate temperature 550 degrees C, deposits 1500A of Poly-Si, and is optical reinforcement from the Poly-Si side 100 - 400 mJ/cm2 It is made to change in between and change of the X diffraction reinforcement from each field at the time of irradiating an ultraviolet radiation pulse laser and making it recrystallize and the mobility of TFT created by the above-mentioned approach is shown. Although Si (111) diffraction peak with the strongest diffraction reinforcement is increasing in proportion to optical reinforcement above threshold energy (about 100 mJ/cm2), other Si (220) and Si (311) diffraction peak are optical on-the-strength 300

mJ/cm2. Augend becomes blunt above and a stacking tendency serves as {111} dominance orientation. 300 mJ/cm2 used as {111} dominance orientation Mobility is increasing rapidly by the above optical reinforcement.
[0012] Next, the crystal stacking tendency of the Poly-Si film which irradiated the ultraviolet radiation pulse laser and recrystallized the surface protective coat deposition and after that like the backward above-mentioned publication which made deposition temperature at the time of depositing in which it is based on a reduced pressure CVD method 500-600 degrees C, and deposited the LPCVD film on drawing 3 is shown. In the LPCVD film deposited at the substrate temperature of 500 degrees C, they are 200 mJ/cm2. With Si film deposited at 520-550 degrees C, they are 400 mJ/cm2 above. {111} dominance orientation is not seen by Si film which became {111} dominance orientation by irradiating a laser beam by the above optical reinforcement, and was deposited at the substrate temperature of 580 degrees C or more.
[0013] Next, the crystal stacking tendency of the Poly-Si film which irradiated the ultraviolet radiation pulse laser to the backward above-mentioned publication which made substrate temperature at the time of depositing on drawing 4 with a reduced pressure CVD method 550 degrees C, shortened assembly time, and deposited the LPCVD film in 400-1500A thickness deposition and after that, and recrystallized the surface protective coat similarly is shown. In 1500A of thickness, they are 400 mJ/cm2. At 800A, they are 300 mJ/cm2 above. At 600A and 400A, they are 200 mJ/cm2 above. It becomes {111} dominance orientation by irradiating a laser beam by the above optical reinforcement.
[0014] The electrical property which the Poly-Si film which makes the main orientation {111} stated by this example has large mobility, is using this for the active region of TFT, and was excellent can be acquired. According to the above, even if the deposition conditions of the LPCVD film differ, the Poly-Si film of {111} dominance orientation is obtained by optimizing the optical reinforcement of exposure ultraviolet radiation pulse laser light.
[0015]
[Effect of the Invention] According to this invention, a thin film semiconductor device with the large mobility of a carrier can be obtained.

[Translation done.]

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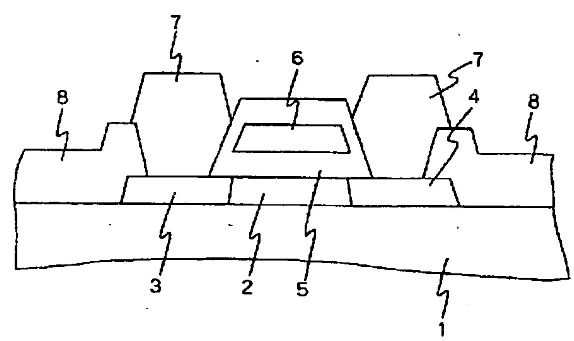
(54)【発明の名称】　レーザアニール方法

(57)【要約】

【課題】キャリアの移動度が大きい薄膜半導体装置を提供する。

【解決手段】絶縁基板上の半導体膜を、レーザアニールを用いることで｛１１１｝配向とする。

図　1



【特許請求の範囲】

【請求項１】絶縁基板と該基板上に形成された半導体膜を有する薄膜半導体装置において、レーザ照射により該半導体層を｛１１１｝面を主体とした配向を持つ多結晶シリコン膜とすることを特徴とするレーザアニール方法。

【請求項２】請求項１記載のレーザアニール方法において絶縁基板上に５５０℃以下の基板温度で減圧ＣＶＤ法により多結晶シリコン膜を形成し、該多結晶シリコン膜をレーザ照射することで｛１１１｝面を主体とした配向を持つ多結晶シリコン膜とすることを特徴とするレーザアニール方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は薄膜半導体装置製造におけるレーザアニール方法に係り、特にアクティブマトリクス方式のディスプレイに好適なレーザアニール方法に関する。

【０００２】

【従来の技術】近年、アクティブマトリクス用の薄膜半導体装置である薄膜トランジスタ（Thin Film Transistor、略してＴＦＴ）材料としては高画質化の点ですぐれている多結晶シリコン(Polycrystalline Silicon, 略してpoly－Ｓｉ）が用いられている。このPoly－Ｓｉ膜は減圧ＣＶＤ法（ＬＰＣＶＤ法）及び常圧ＣＶＤ法（ＡＰＣＶＤ法）により作成されている。絶縁基板としては石英ガラス又は通常のガラス板を用いる。通常のガラス板を用いる際は最高温度が約６４０℃という大きな制約があるためガラス板には熱的影響を与えずPoly－Ｓｉ膜の表面層だけをレーザ照射することで再結晶化する方法が試みられている。この方法によればガラス板に影響を与えない低温熱アニールに比べ結晶性が向上している。

【０００３】従来はこのレーザ照射方法として特開昭60－245124号に記載のようにＳｉ膜で吸収率の大きな紫外光パルスレーザを照射して半導体装置を製造する方法が検討されていた。

【０００４】

【発明が解決しようとする課題】上記従来技術ではレーザ照射によって結晶性を向上させることでＴＦＴ特性を向上させていたが再結晶化したPoly－Ｓｉ膜の結晶の配向性については検討されておらずＴＦＴを作成したときのキャリア移動度を更に向上させる可能性があった。

【０００５】本発明の目的は薄膜半導体装置の特性を向上させるための薄膜半導体装置の構造、とりわけＴＦＴの能動層に使用されるPoly－Ｓｉ膜の配向性を考慮することで更に大きなキャリア移動度を得ることにある。

【０００６】

【課題を解決するための手段】上記目的をガラス基板等の絶縁性基板上に形成された半導体装置であるＴＦＴを構成するPoly－Ｓｉ層を｛１１１｝面を主体とした配向を持たせることにより達成される。

【０００７】このPoly－Ｓｉ層は減圧ＣＶＤ法により基板温度５５０℃以下の温度において１５００Å以下の膜厚で堆積し、５００℃以下で堆積したＳｉ膜では２００ｍＪ／cm² 以上、５２０～５５０℃で堆積したＳｉ膜では４００ｍＪ／cm² 以上の光強度でレーザ光をPoly－Ｓｉ層側から照射することで得られる。又、５５０℃で堆積したＳｉ膜を薄膜化した場合、８００～１５００Åの膜厚では４００ｍＪ／cm² 以上、６００～８００Åの膜厚では３００ｍＪ／cm² 以上、６００Å以下の膜厚では２００ｍＪ／cm² 以上の光強度でレーザ光をPoly－Ｓｉ層側から照射することで得られる。

【０００８】レーザ照射によって再結晶化したPoly－Ｓｉ膜は個々のＳｉ結晶中には欠陥が少なく電子のトラップは粒界に大きく影響される。Poly－Ｓｉの結晶粒界の界面電荷密度は、Ｓｉ単結晶の各結晶面とSiO_2との界面電荷密度が〈１００〉，〈１１０〉，〈１１１〉の順に増加することと同様の関係が成立し、｛１１１｝優位配向のPoly－Ｓｉ膜では配向性の見られないPoly－Ｓｉ膜に比べ膜と垂直方向（〈１１１〉方向）のトラップ密度が大となる。膜と平行方向では反対に｛１１１｝優位配向のPoly－Ｓｉ膜が配向性の見られないPoly－Ｓｉ膜に比べ相対的に低いトラップ密度を示すことになる。トラップ密度が低いと粒界に生じる空乏層幅はせまくなり、ここでのポテンシャル障壁は低くなる。Poly－Ｓｉのキャリア移動度は主として粒界におけるポテンシャル障害の高さで決まる。ＴＦＴのキャリアはPoly－Ｓｉ膜と平行方向に流れる。これらの条件から｛１１１｝優位配向のPoly－Ｓｉ膜では配向性のないPoly－Ｓｉに比べ相対的にキャリアの移動度が大きくなる。

【０００９】

【発明の実施の形態】以下本発明の実施例を説明する。

【００１０】図１は本発明を用いたＴＦＴ全体の断面構造を示す。基板１は歪温度約６４０℃のガラス基板である。基板１を５５０℃に保ち、ヘリウムで２０％に希釈したモノシランガスを原料として圧力１Torrの条件でＬＰＣＶＤ膜を堆積させる。堆積時間は８５分間で１５００Åの膜を堆積させる。次に基板１を４８０℃に保ち、ヘリウムで４％に希釈したモノシランガスと酸素を原料として常圧ＣＶＤにより表面保護膜を約８分間で１０００Å堆積させる。この膜の上面からＸｅＣｌをガス源とした紫外光パルスレーザ（波長３０８ｎｍ，パルス幅２５ｎｓ）を照射することでＬＰＣＶＤ膜を再結晶化しPoly－Ｓｉ膜２，３，４を得る。この時レーザ光強度を４００ｍＪ／cm² 以上とすることでPoly－Ｓｉ膜の主たる配向は｛１１１｝優位配向となり平均結晶粒径は約１０００Åである。次に表面保護膜として用いたSiO_2膜をフッ酸の水溶液で除去する。レーザ照射により再結晶化したPoly－Ｓｉ膜を島状に形成するホトエッチングの工程を通した後、常圧ＣＶＤ法によりゲート絶縁膜用の

ＳｉＯ$_2$ 膜5を堆積させる。次にゲート電極用のPoly－Ｓｉ膜6を５５０℃、1Torrの条件で３５００Å堆積させる。ゲート膜5をホト，エッチした後、ソース，ドレイン領域3，4のインプラを行う。条件はリン（Ｐ）を用い、5×１０^{15}cm^{-2}のドーズ量、３０ＫｅＶの電圧である。リンガラスからなるパッシベーション膜8を４８０℃で５０００Å堆積させ、さらにＮ$_2$ 中６００℃の条件で２０時間以上の熱処理、あるいは２００ｍＪ／cm^2 以上の光強度で紫外光パルスレーザを照射することでインプラ領域を活性化させる。コンタクト用のホト，エッチ行程の後、Ａｌ電極7を６０００ÅスパッタすることでＴ Ｆ Ｔを形成する。

【００１１】図2はPoly－Ｓｉを減圧ＣＶＤ法により基板温度を５５０℃として１５００Å堆積し、そのPoly－Ｓｉ側から光強度を１００～４００ｍＪ／cm^2 の間で変化させ紫外光パルスレーザを照射して再結晶化させた際の各面からのＸ線回折強度と、上記方法で作成したＴＦＴの移動度の変化を示す。最も回折強度の強いＳｉ(１１１)回折ピークはしきいエネルギ（約１００ｍＪ／cm^2 ）以上で光強度に比例して増加しているが他のＳｉ(２２０)，Ｓｉ(３１１)回折ピークは光強度３００ｍＪ／cm^2 以上で増加量が鈍り配向性が｛１１１｝優位配向となる。｛１１１｝優位配向となる３００ｍＪ／cm^2 以上の光強度で移動度は急激に増大している。

【００１２】次に図3に減圧ＣＶＤ法による堆積する際の堆積温度を５００～６００℃としてＬＰＣＶＤ膜を堆積した後上記記載と同様に表面保護膜を堆積、その後紫外光パルスレーザを照射し再結晶化したPoly－Ｓｉ膜の結晶配向性を示す。基板温度５００℃で堆積したＬＰＣＶＤ膜には２００ｍＪ／cm^2 以上、５２０～５５０℃で堆積したＳｉ膜では４００ｍＪ／cm^2 以上の光強度でレーザ光を照射することで｛１１１｝優位配向となり、基板温度５８０℃以上で堆積したＳｉ膜では｛１１１｝優位配向は見られない。

【００１３】次に図4に減圧ＣＶＤ法により堆積する際の基板温度を５５０℃として堆積時間を短くしてＬＰＣＶＤ膜を４００～１５００Åの膜厚で堆積した後上記記載を同様に表面保護膜を堆積、その後紫外光パルスレーザを照射し再結晶化したPoly－Ｓｉ膜の結晶配向性を示す。膜厚１５００Åでは４００ｍＪ／cm^2 以上、800Åでは３００ｍＪ／cm^2 以上、６００Å及び４００Åでは２００ｍＪ／cm^2 以上の光強度でレーザ光を照射することで｛１１１｝優位配向となる。

【００１４】本実施例で述べた｛１１１｝を主配向とするPoly－Ｓｉ膜は移動度が大きく、これをＴＦＴの能動領域に用いることですぐれた電気特性を得ることができる。以上によれば、ＬＰＣＶＤ膜の堆積条件が異なっても照射紫外光パルスレーザ光の光強度を最適化することで｛１１１｝優位配向のPoly－Ｓｉ膜が得られる。

【００１５】

【発明の効果】本発明によれば、キャリアの移動度が大きい薄膜半導体装置を得ることができる。

【図面の簡単な説明】

【図１】本発明のＴＦＴの構造の模式図。

【図２】レーザアニール後のPoly－Ｓｉの結晶性及び移動度の光強度依存性を示す図。

【図３】Poly－Ｓｉ膜の結晶配向性を示す図。

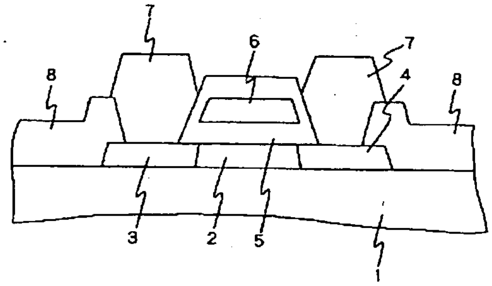
【図４】Poly－Ｓｉ膜の結晶配向性を示す図。

【符号の説明】

１…絶縁性基板、２…多結晶シリコン層、３…ソース領域、４…ドレイン領域、５…ゲート絶縁膜、６…ゲート電極、７…Ａｌ電極、８…パッシベーション膜。

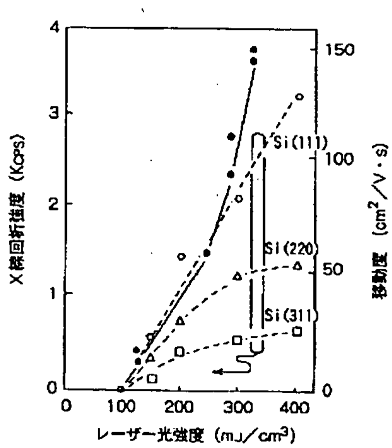
【図１】

図 1



【図２】

図 2



【図3】

光強度(mJ.cm^2) ＼ 成膜温度(℃)	500	520, 550	580, 600
0	アモルファス	アモルファス	{110} 優位配向
200	{111} 優位配向	配向性なし	{110} 優位配向
300	{111} 優位配向	配向性なし	配向性なし
400	{111} 優位配向	{111} 優位配向	配向性なし

図3

【図4】

光強度(mJ.cm^2) ＼ 膜圧(Å)	400	600	800	1500
0	アモルファス	アモルファス	アモルファス	アモルファス
200	{111} 優位配向	{111} 優位配向	配向性なし	配向性なし
300	{111} 優位配向	{111} 優位配向	{111} 優位配向	配向性なし
400	{111} 優位配向	{111} 優位配向	{111} 優位配向	{111} 優位配向

図4

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